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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/736,615	12/14/00	STICKLER H	10007356-1

MM91/1024

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EXAMINER	
ALCALA, J	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 10/24/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/736,615	STICKLER ET AL.	
	Examiner	Art Unit	
	Jose H Alcala	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *7-10 and 12-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Claims 7-10, 13-18 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention and species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 3.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: Reference 144 is not in Figure 4, as disclosed in page 9 line 25. Correction is required.

Specification

3. The disclosure is objected to because of the following informalities: In page 1, lines 4-9, the specification fails to give the serial number of the related US Patent Application, which was filed on the same date as the present application.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5,8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. (US Patent No. 5,449,863).

6. Regarding claim 1, Nakatani teaches a PCSB assembly (See Figure 10A) comprising: a PCSB (The combination of substrate 1 and the other elements of Figure 10A) a first plurality of bus signal trace pairs (Reference number 20, first 6 signal traces from left of Figure 10B) formed in said PCSB; and a second plurality of bus signal trace pairs (Signal traces 7-10 of Figure 10B) formed in said PCSB and positioned next adjacent one another for the entire length thereof (see Figure 10B).

Nakatani fails to explicitly teach that the lines are "low voltage differential" and "small computer system interface". In addition, Nakatani fails to teach that the signal trace pair comprises a RESET signal trace pair, a SELECT signal trace pair and a BUSY signal trace pair. It is well known in the art to use low voltage differential signal traces to reduce noise, in addition Nakatani teaches in column 4, lines 5-7 that the embodiment of the reference, suppresses the noise generated by the fluctuation of potential. The teaching that the traces are "small computer system interface traces", and that there is a RESET signal trace pair, a SELECT signal trace pair, and a BUSY signal trace pair, are all intended use limitations, and it has been held that a recitation with

respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. See Ex parte Masham, 2 USPQ 2d 1647 (1987). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the traces of "low voltage differential" and "small computer system interface", in order to reduce the noise generated by voltage differential for the desired application. It would have been further obvious to one of ordinary skill in the art at the time of the invention, to use the signal traces to transmit any kind of signal desired such as a reset, busy or select signal.

Regarding Claim 2, Nakatani fails to explicitly teach that the minimum spacing of any signal trace pair in said second plurality of signal trace pairs from any signal trace pair in said first plurality of signal trace pairs is about 0.015 in. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make the minimum spacing between any signal trace pair in said second plurality of signal trace pairs and any signal trace pair in said first plurality of signal trace pairs to be about 0.015 in, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claim 3, Nakatani fails to explicitly teach that the minimum spacing between any two adjacent signal trace pairs of said second plurality of LVD SCSI bus signal trace pairs is about 0.008 in. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make the minimum spacing

between any two adjacent signal trace pairs of said second plurality of LVD SCSI bus signal trace pairs to be about 0.008 in, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claim 4, Nakatani fails to explicitly teach that the minimum internal spacing between traces of a signal trace pair of any of said second plurality of LVD SCSI signal trace pairs is about 0.006 in. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to make the minimum internal spacing between traces of a signal trace pair of any of said second plurality of LVD SCSI signal trace pairs to be about 0.006 in, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. See In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding Claims 5 and 8, Nakatani teaches a first exterior surface layer and a second exterior surface layer opposite said first exterior surface layer, and wherein said first plurality of LVD SCSI bus signal trace pairs (Reference number 20 at the top surface) are positioned in said first surface layer and wherein said second plurality of LVD SCSI bus signal trace pairs (Reference number 20 at the bottom surface) are positioned at least partially in said second exterior surface pair. (See Figure 10A, where the first plurality of trace pairs are on the top exterior surface and the second plurality of trace pairs are on the bottom exterior surface).

Regarding Claim 11, Nakatani teaches a PCSB (The combination of substrate 1 and the other elements of Figure 10A) comprising: a first surface layer (top surface of Figure 10A) comprising a plurality of bus signal trace pairs (Reference number 21 at the top of figure 10A); and a second surface layer (bottom surface of Figure 10A) opposite said first surface layer comprising at least a portion of at least one signal trace pair (Reference number 21 at the bottom of figure 10A).

Nakatani fails to explicitly teach that the lines are "low voltage differential" and "small computer system interface". In addition, Nakatani fails to teach that the signal trace pair at the second surface layer comprises a RESET signal trace pair, a SELECT signal trace pair and a BUSY signal trace pair, and excluding all signal trace pairs other than those in said group. It is well known in the art to use low voltage differential signal traces to reduce noise, in addition Nakatani teaches in column 4, lines 5-7 that the embodiment of the reference, suppresses the noise generated by the fluctuation of potential. The teaching that the traces are "small computer system interface traces", and that the signal traces are from the group of: a RESET signal trace pair, a SELECT signal trace pair, and a BUSY signal trace pair, are all intended use limitations, and it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. See Ex parte Masham, 2 USPQ 2d 1647 (1987). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the signal traces of "low voltage differential" and "small computer system interface", in order to reduce the noise generated by voltage

differential for the desired application. It would have been further obvious to one of ordinary skill in the art at the time of the invention, to use the signal traces to transmit any kind of signal desired such as a reset, busy or select signal, and to exclude any unwanted signals.

7. Claims 6, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. (US Patent No. 5,449,863) in view of Leigh et al. (US Patent No. 5,764,489).

Regarding Claim 6, the modification of the Nakatani invention as stated supra for claim 5 teaches all the limitations of the instant claim invention, but fails to teach that the second plurality of signal trace pairs are positioned partially in said first exterior surface layer and partially in said second exterior surface layer. Leigh teaches signal trace pairs (Reference number 14), which are positioned partially in said first exterior surface layer and partially in said second exterior surface layer (See Figure 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references so that the second plurality of signal trace pairs is positioned partially in said first exterior surface layer and partially in said second exterior surface layer, in order to control the impedance of the traces of the printed circuit board.

Regarding Claim 9, the modification of the Nakatani invention as stated supra for claim 8 teaches all the limitations of the instant claim invention, but fails to teach that said second plurality of signal trace pairs are positioned partially in said first exterior surface layer and partially in said second exterior surface layer. Leigh teaches signal

trace pairs (Reference number 14), which are positioned partially in said first exterior surface layer and partially in said second exterior surface layer (See Figure 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the references so that the second plurality of signal trace pairs is positioned partially in said first exterior surface layer and partially in said second exterior surface layer, in order to control the impedance of the traces of the printed circuit board.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references have some of the elements of the instant claimed invention: Gulick et al. (US Patent 5,768,109), Jones et al. (US Patent 5,955,704), Teshome et al. (US Patent 6,236,572 B1), Kanai et al. (US Patent 5,903,442), Horine (US Patent 6,072,699), Novak (US Patent 6,215,372 B1), Dumke (US Patent 6,011,695) and Auerbuch et al. (US Patent 5,308,926).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on (703) 308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

11. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
October 22, 2001